

RESPONSE
SN 09/733,402
PAGE - 2 of 15 -

IN THE CLAIMS:

Please replace the previous claims with the following claims:

Claims 1-26 (Cancelled).

27. (currently amended) A method for programming one or more programmable logic devices, comprising:

programming a first file in a non-native format for programming said one or more programmable logic devices from a remote programmer source;

converting said non-native format programmable logic instructions into a second file having programmable logic instructions in a format native to said programmable logic device;

transferring said second file to a server comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable logic device coupled to a switching circuit;

executing said converted file, for identifying particular target files associated with said programmable logic devices, via a first bus coupled to said switching circuits;

enabling the switching circuit[[s]] corresponding to each programmable logic device having said identified target files via said first bus; and

programming said identified programmable logic devices via a second bus coupled to said switching circuit.

28. (Previously presented) The method of claim 27 wherein said first file is a programmer object file (POF).

29. (Original) The method of claim 27 wherein said remote programmer source is selected from the group comprising a workstation, and a personal computer.

RESPONSE
SN 09/733,402
PAGE - 3 of 15 -

30. (Original) The method of claim 27 wherein said second file is a JAM byte code file.
31. (Original) The method of claim 27, wherein said communications medium is an Ethernet network.
32. (Original) The method of claim 27, wherein said native format comprises a JTAG format.
33. (Original) The method of claim 27, wherein said first bus is a board select bus.
34. (Original) The method of claim 27, wherein said second bus is a JTAG bus.
35. (Original) The method of claim 27 further comprising the step of causing said programmable logic device to enter an initial operating state.

Claims 36-47 (Canceled).

48. (currently amended) An apparatus for programming ~~at least one~~ programmable logic devices, comprising:

~~at least one~~ a plurality of circuit boards, ~~each respectively~~ comprising ~~said at least one~~ a programmable logic device ~~respectively~~ coupled to ~~at least one~~ a switching circuit;

a processor system coupled to said ~~at least one~~ switching circuits on said plurality of circuit boards via a board select bus and a JTAG bus, said processor system for receiving from a remote source, a file in a format native to said ~~at least one~~ programmable logic devices; and

wherein said processor system executes said file in a format native to said ~~at least one~~ programmable logic devices, and identifies particular target files associated with said programmable logic devices and selectively enables said at least one a particular switching circuit corresponding to each programmable logic device having

380573_1.DOC

RESPONSE

SN 09/733,402

PAGE - 4 of 15 -

said target files via the board select bus for programming an said associated programmable logic devices via said JTAG bus.

49. (Original) The apparatus of claim 48 wherein said first and second bus is a backplane.
50. (Original) The apparatus of claim 48 wherein said format native to said remote programmable logic device is a JTAG format.
51. (Original) The apparatus of claim 48 wherein said format native file is a JAM byte code file.
52. (Original) The apparatus of claim 48 wherein said at least one programmable logic device is selected from the group comprising a gate array, field programmable gate array, programmable, field programmable logic array, read only memory, programmed array logic, programmable logic array, and complex programmable logic devices.
53. (Original) The apparatus of claim 48 wherein processor system is a server.
54. (Original) The apparatus of claim 48 wherein processor system is a switch.
55. (New) The method of claim 27 wherein said executing step is via a parallel bus.
56. (New) The method of claim 27 wherein said programming step is via a serial bus.